WHAT IS CLAIMED IS:

1. A behavioral synthesis system, comprising:

a section for generating a control data flow graph from a behavioral description containing a loop process and a non-loop process, using nodes representing processing sections and input/output branches representing data flow; and

a section for automatically synthesizing hardware structure at a register transfer level using the control data flow graph,

wherein a loop process portion of the control data flow graph represents that the nodes contained in the loop process are divided into pipelined stages and processes of the pipelined stages are executed in parallel in each of a plurality of the loop processes, and

the control data flow graph generating section comprises, in the loop process portion, a loop control portion for outputting control signals for executing at least the non-loop process of the loop process and the non-loop process, to the nodes in the stages.

2. A behavioral synthesis system according to claim 1, wherein the loop control portion comprises:

a plurality of ports for outputting the control signals to the nodes in the stages; and

a terminating condition determining node for determining termination, the terminating condition determining node being connected to one or more prescribed ports of the plurality of ports.

3. A behavioral synthesis system according to claim 1, wherein the loop process portion comprises:

a loop port for receiving a prescribed initial value and successively outputting a value obtained by incrementing the input initial value by one per cycle;

a number-of-loops determining node for counting an output from the loop port, determining whether or not the number of loop processes reaches a prescribed number of loop processes, and outputting a result of the determination as a determination output to the loop control portion; and

the nodes in the stages.

4. A behavioral synthesis system according to claim 3, wherein the loop control portion receives the determination output from the number-of-loops determining node, and outputs the control signal for allowing the node

in the stage to execute a non-loop process, from the port of the loop control portion.

5. A behavioral synthesis system according to claim 2, wherein the plurality of ports have a shift register function having the same number of bits as the number of the pipelined stages.

6. A behavioral synthesis system according to claim 5, wherein the plurality of ports supply control signals obtained by successively shifting a prescribed input initial value for each cycle using the shift register function, to the nodes in the stages.

7. A behavioral synthesis system according to claim 1, wherein a node of the nodes in the stages, which has an action external to the loop process portion, is controlled using the control signal from the loop control portion.

8. A behavioral synthesis system according to claim 1, wherein the control data flow graph generating section generates a control data flow graph of a pipelined loop process based on a control data flow graph of an unpipelined loop process.

9. A behavioral synthesis system according to claim 8, wherein the control data flow graph generating section comprises:

a port adding section for newly adding a port at an intersection of a boundary between the stages and a graph branch in the control data flow graph of the unpipelined loop process;

a side-by-side arranging section for arranging the stages to represent parallel processing;

a branch connecting section for connecting a data transfer branch between loops with respect to the stages in the loop process portion; and

a loop control portion adding section for providing the loop control portion in the loop process portion.

10. A behavioral synthesis system according to claim 9, wherein the branch connecting section generates a selector node for selecting one of an initial value provided externally to the loop process portion and a value calculated by the loop process portion and substituting the selected value to a variable in the loop process portion, and

the loop control portion adding section connects

the loop control portion and the selector node so that the control signal output from the loop control portion is used to determine which of the initial value provided externally to the loop process portion and the value calculated by the loop process portion is selected.

11. A behavioral synthesis method, comprising the steps of:

generating a control data flow graph from a behavioral description containing a loop process and a non-loop process, using nodes representing processing sections and input/output branches representing data flow; and

automatically synthesizing hardware structure at a register transfer level using the control data flow graph,

wherein the control data flow graph generating step comprises:

dividing the nodes contained in the loop process into pipelined stages;

generating a loop process portion for executing processes of the pipelined stages in parallel in each of a plurality of the loop processes; and

generating, in the loop process portion, a loop control portion for outputting control signals for

executing at least the non-loop process of the loop process and the non-loop process, to the nodes in the stages.

12. A control program for causing a computer to execute a behavioral synthesis method according to claim 11.

13. A computer readable recording medium storing a control program according to claim 12.

14. A method for producing a logic circuit based on a circuit structure automatically synthesized using a behavioral synthesis system according to claim 1.

15. A logic circuit, comprising:

a loop process portion for repeatedly executing operations in parallel using a plurality of logical operation sections; and

a loop control portion for outputting a control signal for executing at least a non-loop process of a loop process and the non-loop process to at least one of the plurality of logical operation sections,

wherein the loop control portion is provided within the loop process portion.